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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/867,714	05/31/2001	Risto Sepponen	2380-248	6211
7590	11/30/2004			EXAMINER HO, DUC CHI
NIXON & VANDERHYE P.C. 8th Floor 1100 North Glebe Road Arlington, VA 22201			ART UNIT 2665	PAPER NUMBER

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/867,714	SEPPONEN ET AL.
	Examiner Duc C Ho	Art Unit 2665

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 31 May 2001.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-70 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-6,8-19,21-23,26,35-38,40-48,50-63 and 65-69 is/are rejected.
 7) Claim(s) 7,20,24,25,27-34,39,49,64,71 and 72 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 4 & 5.

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

Claim Objections

1. Claims 54-55 are objected to because of the following informalities: Regarding claim 54, if the term "electronic" of "the electronic circuitry" in line 1 is used to refer to the "processing" of the "processing circuitry", it is suggested that the term "processing circuitry" is used for consistency purpose. The same remark applies to claim 55.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(e) that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-6, 8-19, 21-23, 35-38, 40-48, 50-56, 58-63, and 65 –69 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al. (US 6,490,243), hereinafter referred as Tanaka.

Regarding claim 1, Tanaka discloses information data multiplex transmission system, its multiplexer and demultiplexer and error correction encoder and decoder.

forming the payload for the data packet (the formed payload of the mux packet-fig. 3 includes k1, k2, and k3, see col. 25, lines 42-57);

forming the header for the data packet (the formed header of the mux packet-fig. 3 includes the data field H1), *wherein one of the payload and header contains a data field with one or more bits* (the H1 data field includes 11 bits, see col. 26, lines 21-22); and

including in the data packet one or more error correction bits associated with the data field (the H1 data field of the header includes a 3-bits CRC1-fig. 5) *useable by an error correction scheme at a receiver of the data packet to correct an error in the data field* (the transmitted header is decoded at the receiving side-fig. 4, in which passing the H2 through a parity inverter is used as a correction scheme to correct an error in the H1, see col. 25-line 53 to col. 26-line 34).

Regarding claims 12, and 35, these claims have similar limitations as claim 1. Therefore, they are rejected under Tanaka for the same reasons set forth in the rejection of claim 1.

Regarding claim 45, the claim has similar limitations as claim 1. Therefore, it is rejected under Tanaka for the same reasons set forth in the rejection of claim 1. The

transmitting device in figure 1A inherently includes a processing circuitry for forming error correction bits equivalent to the claimed processing circuitry of claim 1.

Regarding claim 59, the claim has similar limitations as claim 45. Therefore, it is rejected under Tanaka for the same reasons set forth in the rejection of claim 45.

Regarding claims 2, 13, 43, 56, and 69, H1-fig.3 is a header data field.

Regarding claims 3, 14, 44, 58, and 68, H2-fig. 3 is a payload data field.

Regarding claims 4, 15, and 36, the H1 field associates with error detection bits CRC1-fig. 5.

Regarding claims 5-6, 18-19, 37-38, 47-48, 63, and 65, in the data field that includes H1 and H2-fig. 11, H2 comprises error correction bits, see col. 27-line 60 to col. 28-line 46.

Regarding claims 8, 17, 40, and 50, a number of bits in H2 field-fig. 3 is used as one or more error correction bits.

Regarding claims 9, 52, in Tanaka the number of bits comes from the H1, and H2 fields.

Regarding claims 10, 22, 41, 51, and 66, in Tanaka the number of bits corresponds to one or more bits in the H1 or H2 of the data packet.

Regarding claims 11, 42, and 53, the CRC bits in Tanaka may vary from 16 to 32 bits.

Regarding claim 16, in Tanaka-fig. 3 the H1 field comprise error detection bits, the H2 field comprises error correction bits for error detection and error correction.

Regarding claim 21, in Tanaka a number of bits in H2-fig.3 are used as the error correction bits.

Regarding claim 23, and 67, in Tanaka the step of passing the field H2 through a parity inverter is an error correction scheme, wherein this step is adaptable to a change in the number of bits used.

Regarding claim 46, the processing circuitry is capable of forming the data packet with H1-fig. 3 field including one or more error detection bits.

Regarding claim 54, the circuitry and the transmitter of the transmitting device figure 1A is locatable in a stationary radio network node.

Regarding claim 55, the circuitry and the transmitter of the transmitting device figure 1A is locatable in a mobile radio network node.

Regarding claim 60, the circuitry of Tanaka is inherently configured to detect the error detection bits of the H1 field, which associates with error detection bits CRC1-fig. 5.

Regarding claim 61, the circuitry of Tanaka is inherently configured to used the H1 field-fig. 3 for error detection bits, wherein the H2 field comprises error correction bits for error detection and error correction.

Regarding claim 62, the circuitry of Tanaka is inherently configured to use a number of bits in H2 field-fig. 3 for one or more error correction bits.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 57, and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka, in view of Honkasalo et al.(US 6,636,497), hereinafter referred to as Honkasalo.

Regarding claim 57, Tanaka discloses all claimed limitation, except the data field indicates a transport format for the data packet.

Honkasalo discloses an air interface capacity scheduling method. Referring to figure 3, a Transport Format Indicator (TFI) 304 tells the receiver the transport formats of a different transport channels, see col. 6-line 66 to col. 7-line 24.

One skill in the art would recognize the advantage of using a TFI field indicating a transport channel in a data structure, which enables monitoring of a set of parameters of the transport format such as a current transmission rate of a channel.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Tanaka with Honkasolo.

The suggestion/motivation for doing so would have been to monitor a set of parameters of a transport format such as the current transmission rate of a channel.

Therefore, it would have been obvious to combine Honkasolo with Tanaka to obtain the invention as specified in claim 57.

Regarding claim 70, the claim has similar limitations as claim 57. Therefore, it is rejected under Tanaka for the same reasons set forth in the rejection of claim 57.

8. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka, in view of Kalliojarvi (US 6,438,723).

Regarding claim 26, Tanaka discloses all claimed limitations, except (1) a transport format indication field including one or more bits indicating a transport format for the data packet.

Kalliojarvi discloses a method and arrangement for the reliable transmission of packet data. In the context of digital cellular communication system of the third generation employing WCDMA, a frame of 10ms consisting of 1280 QPSK symbols, i.e. 2560 bits would have its control information to include transport format indicator and packet header taking about 10 to 15 percent of symbol capacity, see col. 10, lines 47-60. In other words, the transport format indicator information can also be expressed in terms of bits or symbol capacity, see also col. 7-line 12 to col. 11-line 16 (corresponding to (1)).

Further, in Kalliojarvi each superpacket could fit exactly into a frame, and comprises of CRC bits for error detection and error correction at a receiving side, see col. 10- line 47 to col. 11-line 16.

One skill in the art would recognize the advantage of using a mechanism in which the error correction bits associated with the transport format information into the system of Tanaka such that errors in a superpacket can be detected for correction at the receiving side.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Tanaka with Kalliojarvi.

The suggestion/motivation for doing so would have been to provide error correction for transmitted information including the transport format indicator at the receiving side.

Therefore, it would have been obvious to combine Kalliojarvi with Tanaka to obtain the invention as specified in claim 26.

Regarding claim 54, please see the rejection of claims 2 and 26.

Allowable Subject Matter

9. Claims 7, 20, 24-25, 27-34, 39, 49, 64, and 71-72 are objected to as being independent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dahlin et al.(US 5,142,539); Naden et al.(US 6,560,206); Wantanabe et al. (US 6,084,888) are cited to show error corrections of important fields in data packet communications in a digital mobile radio network, which is considered pertinent to the claimed invention.
11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc Ho whose telephone number is (571) 272-3147. The examiner can normally be reached on Monday through Friday from 7:00 am to 3:30 pm.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (571) 272-3155.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-2600.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2665

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patent Examiner



Duc Ho

11-03-04